WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP

ABSTRACT OF THE DISCLOSURE

A delay locked loop apparatus includes a first delay element to receive a reference signal, to delay the reference signal by a delay time, and to output a first delayed signal. A second delay element is used to receive the first delayed signal, to delay the first signal delayed signal by the delay time, and to output a second delayed signal. Also included is a harmonic lock prevention circuit to receive the reference signal, the first delayed signal, and the second delayed signal, and to adjust the delay time so that a period of each delayed signal is within a predetermined range.